CE1901 LABORATORY PROJECT

SUMMARY

Glitches in signal voltage can occur when propagation delays through different circuit paths cause a temporary incorrect output voltage after the input changes. These short pulses could cause incorrect behavior in circuits connected to the signal. The hazard to the system or user depends on the type of circuit connected to the signal.

PRELIMINARY READING

Glitches in output signal voltage occur when changes to the inputs cause a temporary incorrect output voltage because of different propagation delays through the circuit paths. These short pulses could cause incorrect behavior in circuits connected to the signal. This incorrect behavior is called a **hazard**. The hazard to the system or user depends on the type of circuit connected to the signal. Two types of circuits could be connected to the glitching signal. An **asynchronous circuit** is a circuit that responds immediately the signal change. A **synchronous circuit** is a circuit that samples the signal only at a time controlled by a sample clock. Figure 1 diagrams both types of circuit.

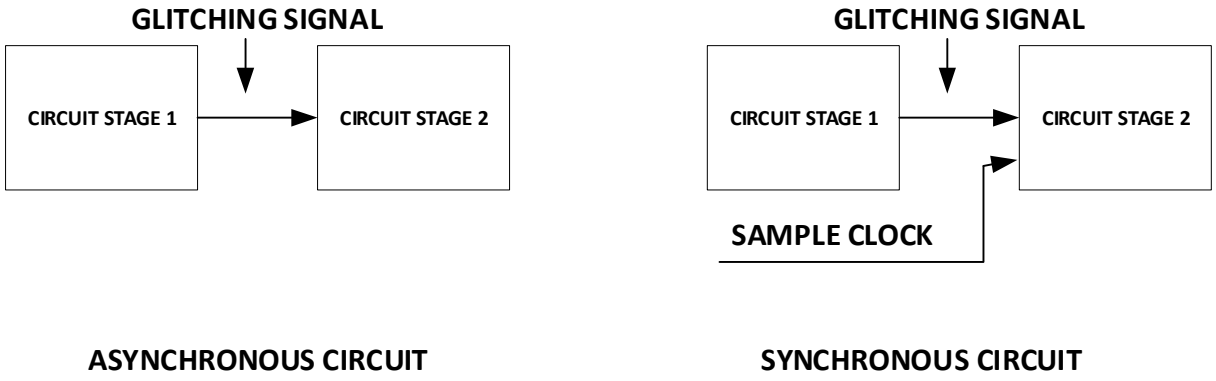

Figure 1: Comparing asynchronous and synchronous circuits

Synchronous circuits solve the glitch problem by increasing the period of the sample clock so that it exceeds the total propagation delay of the glitching circuit. This allows the glitch to disappear before the signal is sampled. Asynchronous circuits respond immediately to the glitch and hazard-free design techniques must be used to remove glitches if circuit stage two is an asynchronous circuit.

The logic waveform of a glitch shows a brief transition away from its final value. In two-level sum-of-product circuits, the common glitches are called **static 1-hazard** and **static 0-hazard**. They are named **static** because the output should have stayed stable, or static, and did not. These glitches represent signals that should remain static at logic-1 and logic-0 but instead incorrectly transition through an incorrect voltage. Figure 2 compares these common hazards. The figure shows a logic waveform and an example of what is often seen on an oscilloscope.

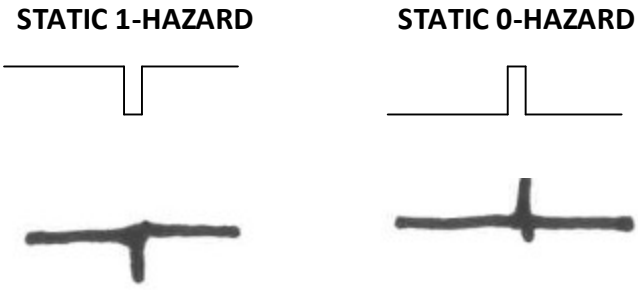

Figure 2: Comparing static 1-hazard and static 0-hazard

Hazard-free design requires an analysis of circuit path lengths to determine if a hazard might exist. A hazard exists when any one-bit change might result in a shorter path changing the output before the longer path restores it. Consider a function F(ABCD), its K-map, and its minimized circuit. The design is shown in Figure 3.

$$F(ABCD) = \sum_m (1,3,5,7,8,9,12,13)$$

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	**1**	**1**	0
$\bar{A}B$	0	**1**	**1**	0
AB	**1**	**1**	0	0
$A\bar{B}$	**1**	**1**	0	0

$$F(ABCD) = A\bar{C} + \bar{A}D$$

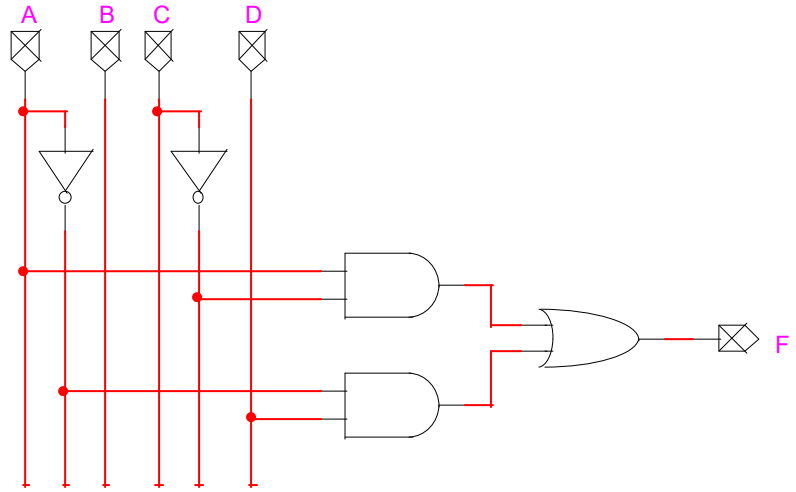

Figure 3: Design of logic equation with potential glitches

Because the logic-1 terms are grouped in the K-map, analysis looks for moments of time when the output should stay at a logic-1 but instead glitches to a logic-0. ***Standard practice is to look only at one input bit changing at any time*** across all possible logic-1 → logic-1 transitions. The hazard exists when a one-bit input change causes a move between prime implicant AND-gates. Table 1 shows all the transitions for the logic-1 minterms of this circuit.

Table 1: Hazard Minterm Transition Identification

MINTERM TRANSITION	GATE COVERING TRANSITION
1 → 3	$\bar{A}D$
1 → 5	$\bar{A}D$
1 → 9	$\bar{A}D \rightarrow A\bar{C}$
3 → 1	$\bar{A}D$
3 → 7	$\bar{A}D$
5 → 1	$\bar{A}D$
5 → 7	$\bar{A}D$
5 → 13	$\bar{A}D \rightarrow A\bar{C}$
7 → 3	$\bar{A}D$
7 → 5	$\bar{A}D$
8 → 9	$A\bar{C}$
8 → 12	$A\bar{C}$
9 → 1	$\bar{A}C \rightarrow A\bar{D}$
9 → 8	$A\bar{C}$
9 → 13	$A\bar{C}$
12 → 8	$A\bar{C}$
12 → 13	$A\bar{C}$
13 → 5	$\bar{A}C \rightarrow A\bar{D}$
13 → 9	$A\bar{C}$
13 → 12	$A\bar{C}$

Not all these transitions will cause glitches. The next step is analyzing the timing behavior of each one to see if a glitch occurs. Figure 4 shows the results for two of these transitions: 5 → 13 and 13 → 5.

Figure 4: Timing waveforms for two of the hazard transitions

The transition from 5 → 13 does not cause a glitch because at least one of the OR gate inputs is always logic-1. The transition from 13 → 5 does cause a glitch because there is a range of time where both OR gate inputs are logic-0. This is caused by difference in the delay paths of the two OR gate inputs. Hazard-free design requires the addition of a consensus term AND gate for the transition 13 → 5. Analysis will also show that the hazard from 9 → 1 also causes a glitch. **This laboratory is designed to help you visualize glitches but not to correct them.**

PRE-LABORATORY WORK

Complete a Quartus schematic design and simulation for the K-map minimized function of F(ABCD) = Σm(4,6,9,11,12,13,14,15). **In simulation, use** a Gray code count pattern rather than standard binary. Be sure to include all four inputs bits even if some of them do not appear in the final equation. Gray code only changes one bit per count while standard binary changes multiple bits per count. **Note** that you will not see glitches in Quartus simulation because Quartus simulation assumes ideal gates with no delay. **Use** simulation only to verify you have a functioning design.

DELIVERABLES DUE DURING THE LABORATORY PERIOD

Each student team must complete these deliverables. Individual work is also allowed.

1. **Check out** a breadboard, wire kit, Analog Discovery instrumentation kit, and appropriate 74LS00 family chips from EECS Tech Support. Consider the 74LS04, 74LS08, 74LS32, and 74LS51.
2. **Build** and **demonstrate** a working circuit.
    a. **Focus** on using the shortest wires possible. **Consider** red = power, black/white/gray = ground, yellow = inputs, green = outputs.
    b. **Use** Patterns to generate a Gray code count sequence on input bus ABCD.
    c. **Use** Logic to visualize the output F. **Note** that you will not see glitches using logic because the logic analyzer is a sequential second stage circuit.
    d. **Verify** that the circuit is built correctly by comparing the minterm values against the desired output.
    e. **Grab** a screenshot of the waveform diagram showing correct operation.
3. **Next** visualize glitches using the oscilloscope. The o-scope is not a synchronous circuit.
    a. **Add** a connection between the most significant input bit, A, and o-scope channel 1. **Do not remove A from your circuit!**
    b. **Move** the F output signal to o-scope channel 2.
    c. **Visualize** any minterm transitions that are causing glitches.
    d. **Grab** a screenshot of the o-scope diagram showing glitches occurring.

4. **Complete** a laboratory submission packet.
5. **Submit** your laboratory packet using the method required by your instructor.